PROJECT PROFILE

2A713: Highly optimised design methods for yield and reliability (HONEY)

EDA FOR SOC DESIGN AND DFM

Partners:

Dolphin
IMEP (Institute of Microelectronics, Electromagnetism and Photonics)
IMMS (Institute of Microelectronic and Mechatronic Systems)
Infineon
Infiniscale
MunEDA
STMicroelectronics
X-FAB
Xyalis

Project leader:

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Key project dates:

Start: July 2007
End: December 2010

Countries involved:

France
Germany
Italy

Integrated circuits require enhanced trade-offs between targeted performance and risk of failure. Early in the design flow, yield and reliability-oriented methodologies must be implemented to guarantee that long-term circuit operation is in-line with specs. The main objective of the HONEY project is to improve yield and reliability for ever smaller but higher performing chips without affecting the fundamental silicon process. A leap in design for manufacturing will speed production ramp-up to economically acceptable levels. This will boost Europe's global position in a range of applications that include complex system-on-chip devices for automotive, communications and consumer electronics.

As integrated circuit (IC) dimensions become ever smaller, both environmental and operating conditions have a major influence on chip quality and reliability. A crucial challenge in designing high-performance analogue and mixed analogue-digital signal (AMS) circuits using leading-edge nanotechnologies is to predict and mitigate the influence of a range of dynamic factors, such as temperature, stress and aging. This requires new design strategies that take account of yield and lifetime-reliability models within a dynamic operating conditions concept.

Major headaches for chipmakers

Yield and reliability difficulties are major headaches for semiconductor manufacturers. As circuit dimensions reduce from one generation of CMOS technology to the next and circuit complexity increases, especially with the development of complete system-on-chip (SoC) devices, there are major increases in parameter dispersions caused by process variations and optical distortions from layout to lithography.

Yield troubles are principally:

- **Functional losses:** chips failing to run at all – a problem that has grown rapidly, from less than 5% at 350 nm CMOS nodes a decade ago to more than 60% for 65 nm nodes now. These losses come from spatial or pattern changes, caused by variations in metallisation width and thickness or mask misalignment during the manufacturing process, and from random sources such as particle contamination that lead to short or open circuits; and
- **Parametric losses:** where a chip works but does not meet its design specification. This appears, for example, when the chip is too slow or too hot. This can come from random variations during fabrication that contribute to threshold voltage problems, high leakage currents, interconnect parasites, etc. or affect dynamic power consumption and operating temperature. Environmental variations may also be a factor.

In addition to such yield losses that become apparent at the end of the chip-fabrication process, performance and functionality may also degrade during the entire operational lifetime of the chip. This unavoidable limitation on reliability is caused by different kinds of aging mechanisms resulting

from basic physical effects within devices and interconnects.

Two clearly separated kinds of failure rate appear over the product lifetime. The early failure rate peaks almost at the very beginning, usually followed by a quick downturn that is expected to level off well below the required reliability value. However, the failure rate eventually increases again as a result of wear-out mechanisms. Here, the main issue is to pass a critical threshold value as late as possible to guarantee long IC operating times.

Innovative design techniques

The MEDEA+ 2A713 HONEY project is focusing on obtaining yield and reliability improvements through innovative design techniques in terms of redundancy, high yield libraries, yield-oriented design optimisation, place-and-route tools and post-layout optimisations. These solutions will offer yield-loss prevention and recovery throughout the whole design flow.

Design for reliability (DfR) is a consequent complement to design for yield (DfY); HONEY offers the opportunity to follow the same statistical-type approach for both to propose new generic solutions. Implementations will address 65 and 45 nm nodes principally, with a retrofit to 90 nm and experiments on 32 nm.

Consortium members include three main European chipmakers, led by STMicroelectronics, together with four computer-aided design (CAD) equipment vendors and two research institutes.

Innovations are proposed in:

1. Block design, including: adapting built-in self-repair know-how in memory design to logic circuits; analysis of sizing rules and design constraints regarding feasible and functional designs; nominal constraint and performance analysis and optimisation for AMS circuits; enhanced statistical analysis and optimisation methodologies for AMS circuits and digital library cells based on statistical process modelling; design for manufacturing and design for manufacturability (DfM) compliant libraries for high-yield SoC devices; and moving DfM/DfY upstream to create a design that is as easy to manufacture and high yielding as possible;
2. Automated layout generation and optimisation, including: introduction of model-based techniques into the routing domain; extending DfM techniques to design for printability; automatic 3D analysis of wafer surfaces; impact of layout defect specifications on specific lithographic processes; layout optimisation versus process-specific chemical mechanical polishing; and achieving a high level description to physical layout flow in which all design and analysis stages are DfM/DfY aware; and
3. Process maturity monitoring through predictions and measurements, including: yield prediction to monitor the fabrication process, showing which defect types cause most yield loss, determining the extent of parametric problems and determining the overall production cost of a new chip before starting actual fabrication; higher abstraction levels for mitigating process variability and aging; test chips for fast evaluation of process maturity; optimising yield concurrently with other traditional design metrics; and enabling a reliability-aware design process in all development phases, minimising or balancing stresses and thermal loads and/or reducing sensitivity to these stresses or loads.

Boosting competitiveness

Work in the project will improve convergence between its industrial, CAD and academic partners on yield and reliability modelling, measurement techniques and process variations. Integration of models and tools will be performed in standard electronic design automation (EDA) environments and languages. Embedded diagnostic systems will be standardised to offer and guarantee further process efficiency.

HONEY will result in a consistent yield- and reliability-oriented design flow from block and library levels, down to layout and mask-making levels. It will target necessary trade-offs between performance and risk of failure with defect cost, area cost, power and speed as key parameters.

Success will bring about a methodology leap in circuit yield and reliability and efficient use of production equipment, leading to faster and more economic ramp-up of new production by European chipmakers. The new methods will be exploited immediately by participating industrial partners. And CAD vendors involved will be able extend their product ranges in terms of yield-oriented flows and modules.

The result will be shorter time to market for lower cost and more reliable chips. This will improve European competitiveness in the global market and boost employment both directly and in the wide range of industries – from transport to communications – that rely on microelectronics.

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